
# DESIGN OF AN ANALOGUE FRONT-END FOR SIPM

## Supervisor:
## Prof. Christophe De la taille

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Yiming Wei

ÉCOLE POLYTECHNIQUE

INSTITUT POLYTECHNIQUE DE PARIS

ΩMEGA Microelectronics

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# 1 INTRODUCTION

## 1.1 SiPM in particle and nuclear physics

The discovery of gamma-ray emissions in 1967 by the OSO III satellite marked the inception of high-energy gamma-ray astronomy, a field that has since burgeoned into a vital discipline for probing the most energetic phenomena in the universe. The very high-energy (VHE) electromagnetic radiations that reach Earth, detectable by contemporary telescopes, have unveiled the existence of VHE phenomena pervading the cosmos, raising questions that demand more refined data for a deeper understanding. The Cherenkov Telescope Array (CTA) project emerges as a monumental leap in this quest, designed as a more advanced observatory to delve deeper into these enigmatic phenomena. By employing telescopes of various sizes, the CTA aims to provide an unprecedented dynamic range of gamma-ray energies, with Large Size Telescopes (LSTs) targeting the detection of lower energy gamma rays ever observed by ground-based instruments (in Fig.1).

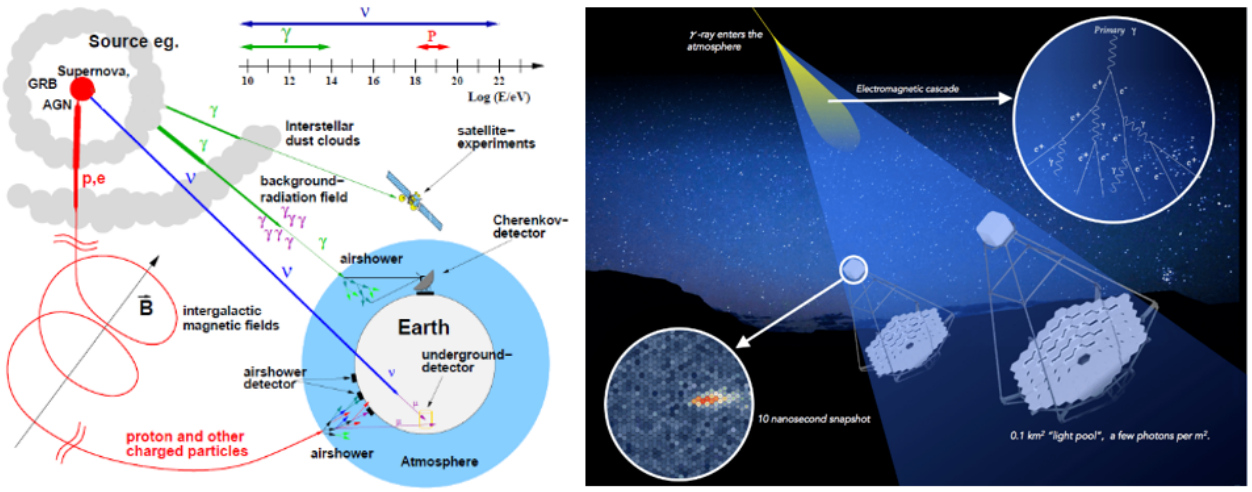


Figure 1: The journey of the cosmic rays from their source to their detection. Reprint from [1][2].

The core of this advancement hinges on the utilization of Silicon Photomultipliers (SiPMs), a novel technology in photosensors, being explored to outfit a new generation camera for the CTA telescopes called CITIROC[3]. SiPMs are anticipated to significantly enhance the sensitivity of the telescopes to as low as possible energies, around 10 GeV, higher photodetection efficiency, compactness, and robustness against magnetic fields, promising to lower the energy threshold for gamma-ray detection.

In High Energy Physics (HEP) experiments, the quest to explore subatomic realms involves accelerating particles to high energies for collisions, creating new particles from energy conversion. This process produces short-lived particles, detectable only through the decay products they leave behind. To capture these events, sophisticated tracking and vertex detectors are employed near the collision points, designed to map the trajectories of these emergent particles accurately. These detectors, embedded within magnetic fields, leverage pixelated layers for detailed track reconstruction, pivotal for identifying rare physics phenomena and enhancing collision rates. As the challenges of probing the subatomic world grow, the advancement in pixel sensor technology becomes increasingly crucial, directly influencing the precision and capability of future HEP explorations[4].

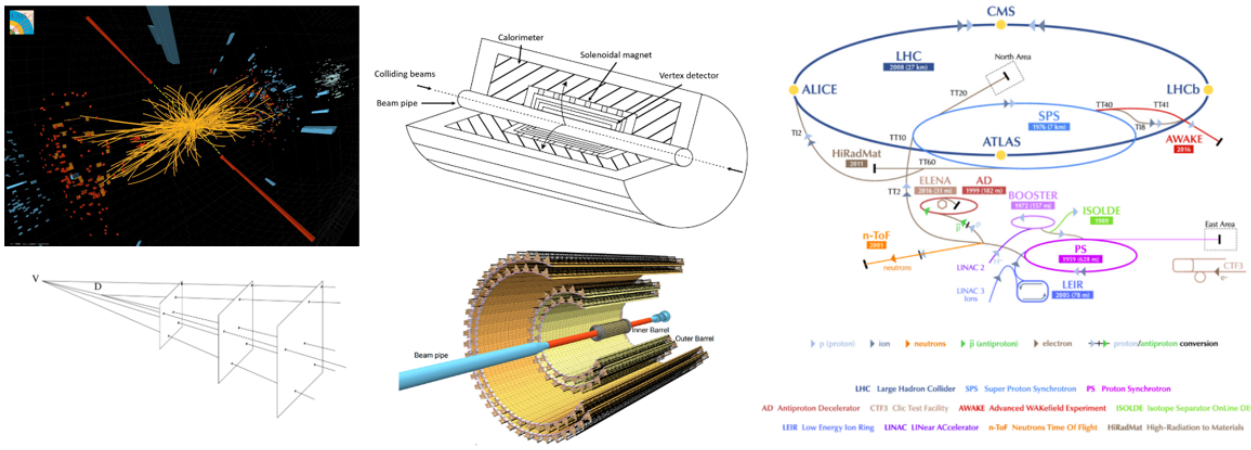


Figure 2: (Left) Topology of a short-lived particle decay.(Middle) Schematic view of an ALICE ITS layout. (Right) An overview of the accelerator complex at CERN and the experiments within it. Reprint from [5] [6][7].

## 1.2 SiPM in medical and biophotonics imaging

Positron Emission Tomography (PET) is a type of nuclear imaging technique that utilizes gamma photons emitted from positron decay to produce three-dimensional images depicting the body's functional processes. Its primary uses are in clinical research, oncology, and studying brain functions. Unlike other imaging methods, PET provides unique insights into the body's metabolism by employing radioactive substances, known as tracers, to identify the location of cancerous cells within the body.

Before undergoing a PET scan, a patient receives an injection of a radiolabeled compound (commonly Fluorodeoxyglucose, or FDG), which is integrated into a biologically active molecule. This molecule is then absorbed by tissues affected by disease, preparing the patient for imaging. As the radioactive tracer decays, it emits a positron that travels a short distance (between 0.1 and 1 mm) in the body before colliding with an electron, resulting in the annihilation of both particles and the release of two gamma photons in opposite directions (180° apart). These photons are detected by a circular array of detectors that convert the gamma

photons into visible light, which is then captured by either photomultiplier tubes (PMTs) or silicon photomultipliers (SiPM).

The PET scanner's role is to accurately detect these photon pairs to establish the Line of Response (LOR), which indicates where annihilation occurred. This involves determining the photons' energy, position, and time of arrival. The data collected is processed by a coincidence unit that filters out non-coincident photons (outside a narrow time window) and uses the remaining information to construct LORs. From numerous LORs, a comprehensive 3-D tomographic image is generated, pinpointing the location of the tracer accumulation and, consequently, the tumor cells.

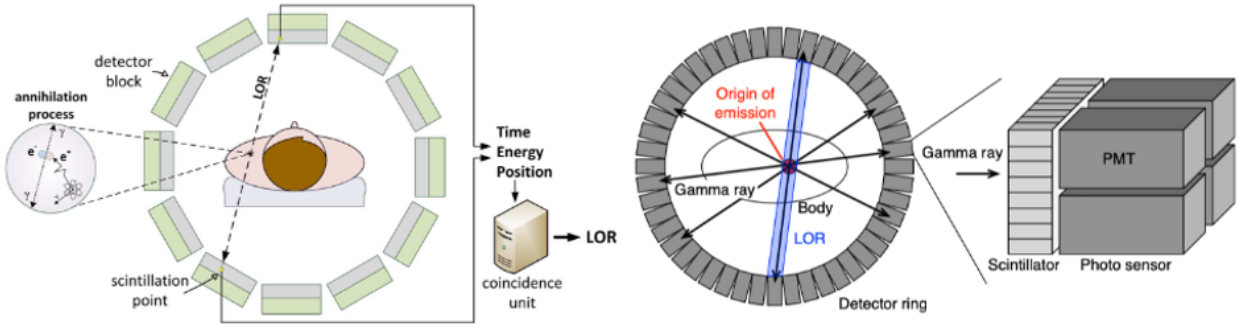


Figure 3: PET working principle and scanner. Reprint from [8].

As technology advances, when the coincidence timing resolution of a system is reduced to several hundred picoseconds, it becomes possible to estimate the region where an annihilation event occurs along the LOR by measuring the time difference of the light's flight. This technique is known as Time-of-Flight (TOF) technology. As illustrated in Fig.4, unlike traditional PET, which can only determine that an annihilation event occurred somewhere along a specific LOR, TOF-PET can pinpoint the specific area on the LOR where the annihilation event took place.

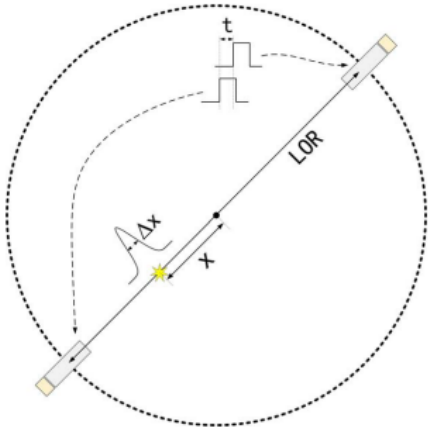


Figure 4: ToF-PET working principle. Reprint from [9].

Fluorescence Lifetime Imaging Microscopy (FLIM) is a technique that measures the decay time of fluorescence from a fluorescent sample. This decay time can reveal information about the environment of the fluorophore molecule, such as its interactions with other molecules, changes in pH, or other factors that can affect its quantum yield or energy transfer processes.

The core principle of FLIM is that when a fluorophore is excited by a photon, it doesn't emit its fluorescence instantaneously but rather after a characteristic 'lifetime.' By measuring this lifetime across different points in a sample, FLIM can create an image based on the spatial distribution of these lifetimes.

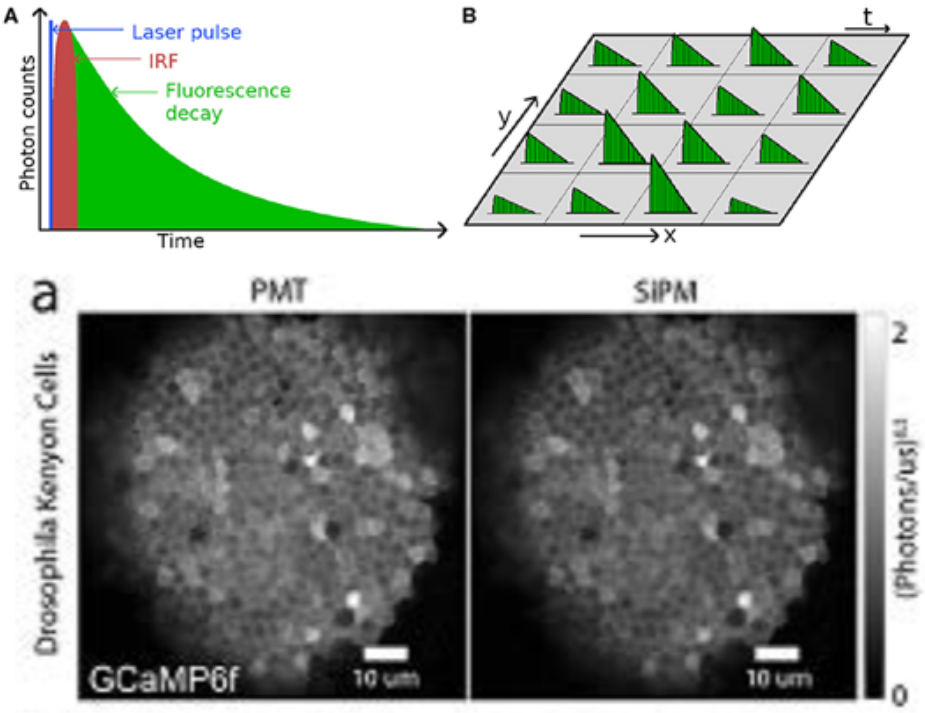


Figure 5: Basic principle of FLIM and Simultaneous raster-scanning calcium imaging with a PMT and blue-sensitive SiPM. Reprint from [10][11].

SiPM have improved FLIM applications significantly. Due to their high photon detection efficiency, they can provide more accurate measurements of fluorescence lifetimes, especially at low light levels. SiPMs detect single photons and generate a corresponding electronic signal. Each microcell within an SiPM operates above a breakdown voltage and can independently start an avalanche process when a photon is detected, leading to a measurable current pulse. This makes SiPMs highly sensitive and capable of detecting photons with high temporal resolution, which is crucial for accurately timing the arrival of photons and thus determining the fluorescence lifetime[10][11][12].

## 1.3 SiPM in LiDAR

LiDAR, which stands for Light Detection and Ranging, is a remote sensing technology that measures distance by illuminating a target with a laser light and analyzing the reflected pulses. This technique relies on the time-of-flight principle to determine the precise distance to an object, creating detailed 3D representations of terrain and surfaces(in Fig.6).

SiPM greatly enhance LiDAR systems by offering high sensitivity to light, which allows for the detection of single photons and extends the system's range. Their excellent timing resolution leads to more accurate distance measurements, enabling finer detail in 3D modeling[13]. SiPMs are less affected by ambient light due to their compatibility with optical filters, and their ability to work with eye-safe infrared light makes them suitable for widespread use, including in safety-critical applications.

The use of SiPMs in LiDAR technology is beneficial for various applications, such as creating detailed maps for geological surveys from airborne platforms and providing high-resolution environmental data for autonomous vehicles[14]. This makes SiPMs integral to improving the performance and safety of LiDAR-based systems[13].

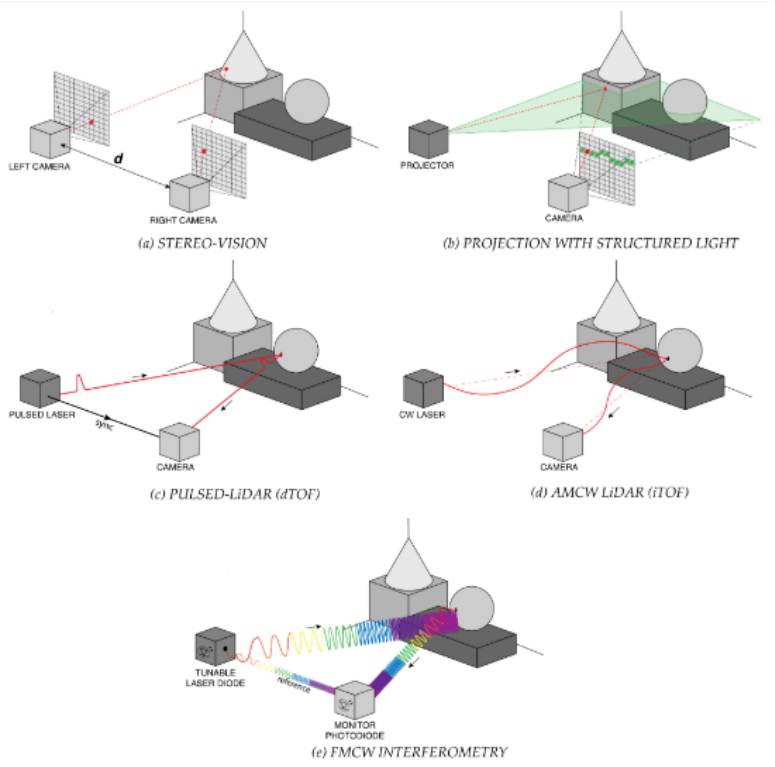


Figure 6: Schematic representation of some 3D ranging techniques: (a) stereo-vision, (b) projection with structured light, (c) pulsed-LiDAR (dTOF), (d) amplitude-modulated continuous-wave (AMCW) LiDAR (iTOF), and (e) frequency-modulated continuous-wave (FMCW) interferometry. Reprint from [13][15].

# 2
# SIPM ELECTRICAL MODEL

## 2.1 PMT

A Photomultiplier Tube (PMT) is a type of vacuum tube equipped with a light-sensitive component called a photocathode, typically made of semiconductor material. When photons interact with the photocathode, electrons are emitted into the vacuum. The photocathode is maintained at a high negative voltage, often up to -1000 volts, relative to the anode, which is the electrode that collects the signal. This setup creates a strong electric field within the tube.

To amplify the initial photoelectron, the PMT uses a series of dynodes arranged in a cascade. Each dynode is set at a successively higher potential than the last, thereby attracting the electrons and inducing secondary electron emissions upon impact. A resistive voltage divider, fed from a high voltage power supply, establishes the potential difference across the dynodes.

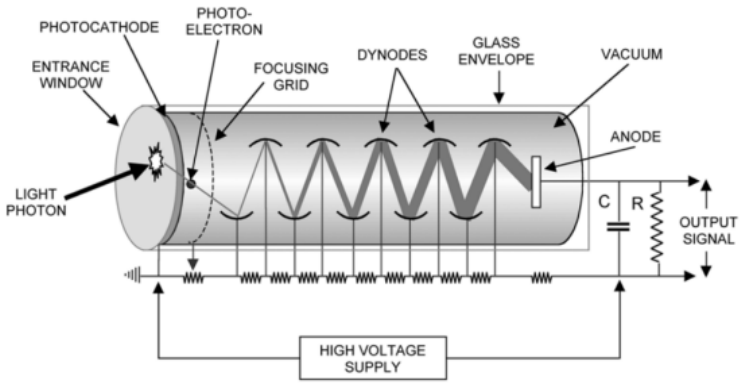


Figure 7: Schematic of a PMT . Reprint from [16].

One of the limitations of PMTs is their power consumption. For the device to maintain a linear response—where the output current increases proportionally with the number of detected photons—the current through the resistive divider must be significantly greater than the tube's photocurrent. This is to ensure minimal voltage drop across the dynodes as the photocurrent varies. As a result, PMTs consume a considerable amount of power when operating.

The multiplication process of the electrons culminates at the anode electrode, where the amplified current pulse is collected. In a PMT, the electron multiplication process concludes naturally within a few nanoseconds, resulting in a very fast signal output.

## 2.2 SiPM

A Silicon Photomultiplier is comprised of a grid of micro-cells, each containing an Avalanche Photodiode (APD) in series with a quenching resistor. In contrast to the PMT, a SiPM is a solid-state sensor, with micro-cells typically measuring 50$\mu$m by 50$\mu$m. SiPMs operate by reverse-biasing the diode – positive voltage is applied to the N-doped region (cathode), relative to the P-doped region (anode).

The bias voltage is set sufficiently high to trigger an avalanche breakdown: the electric field is so powerful that it imparts enough kinetic energy to charge carriers to create additional electron-hole pairs via the avalanche effect.

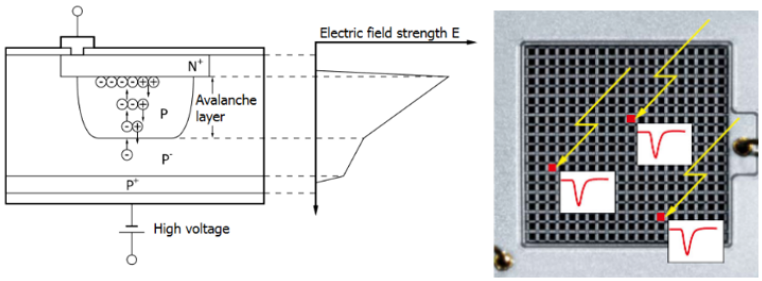


Figure 8: (Left)2D-cut of an Avalanche Photo Diode. (Right) Photon counting with a SiPM . Reprint from [17].

As with PMTs, APDs in a SiPM have a gain that depends on the bias voltage. However, SiPM APDs work in Geiger mode, meaning the bias voltage is beyond the photodiode's breakdown voltage (with a typical overdrive of 3V). This mode of operation does not maintain a linear relationship between the number of initial photoelectrons and the total charge at the anode electrode. Each APD behaves like a digital detector, producing a current pulse upon the detection of at least one photon. When multiple APDs are arrayed in parallel (as in a SiPM), the cumulative current can serve as an approximation of the incident photon count.

Unlike PMTs, where the avalanche process concludes spontaneously, SiPMs integrate a quenching resistor in every cell to automatically limit the current, allowing the device to return to a stable state after pulse generation. The SiPM operation can be summarized in two phases:

1. **Avalanche Phase:** The photon detection initiates an avalanche, modelled by the closure of a switch. The photodiode's depletion capacitance $C_d$, charged to the bias voltage $V_{BIAS} > V_{BD}$, discharges through a low resistance $R_S$. The avalanche ceases when the voltage across $C_d$ approaches the breakdown voltage $V_{BD}$, and the current reaches its peak value: $I_{max} = \frac{V_{BIAS} - V_{BD}}{R_q}$.

2. **Quenching and Reset Phase:** The quenching resistor $R_q$ curtails the current, leading to a voltage drop that recharges the depletion capacitance at a slower rate. This larger time constant governs the reset phase, priming the SiPM for subsequent photon detection.

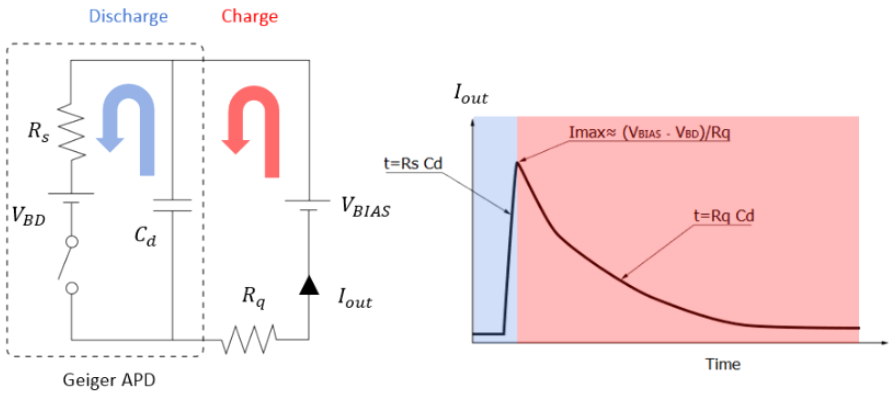


Figure 9: Basic 2-steps operation of a SiPM. Reprint from [18].

This functional cycle allows the SiPM to act as an efficient photon detector, with each micro-cell primed for rapid photon event responses, while the array collectively provides a photon count estimate.

If there is no inductor in the circuit (only resistance R and capacitance C), the rise time of the signal is very fast, and the signal amplitude is determined by the charge Q divided by the capacitance C (Q/C). The decay time of the pulse is controlled by the RC time constant of the circuit. When inductance is taken into account in Fig.10, the rise time of the signal starts to degrade due to the inductive effect, which opposes the change in current. This inductive effect introduces an L/R time constant, which slows down the rise of the pulse. If the resistance is reduced further, say to 5 ohms without inductance, the discharge of the SiPM becomes faster, resulting in a shorter pulse. This is beneficial for applications like LIDAR readout, where double pulse separation is important. Adding even a little more inductance can lead to the circuit behaving as an RLC (resistor-inductor-capacitor) circuit, which affects the rise time negatively. This RLC circuit can start oscillating(blue line Fig.10), which is not desirable for high-frequency applications, as it can cause signal degradation.

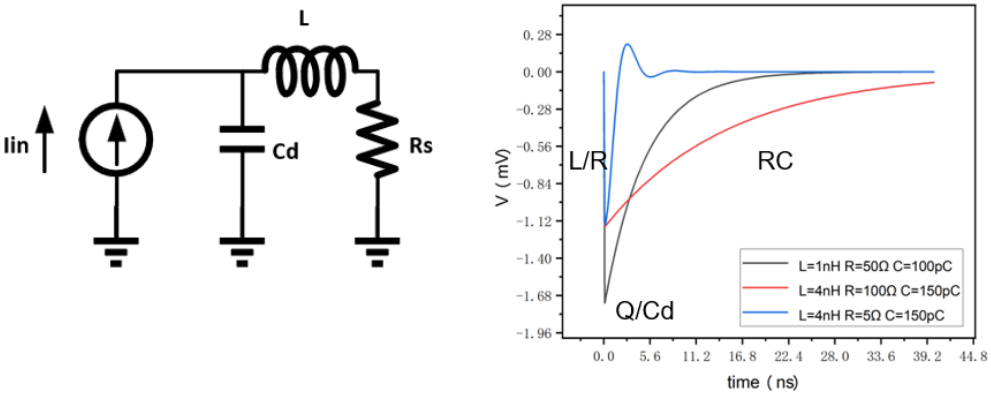


Figure 10: Model of a SiPM taking account of parasitic inductance.

## 2.3 Corsi model

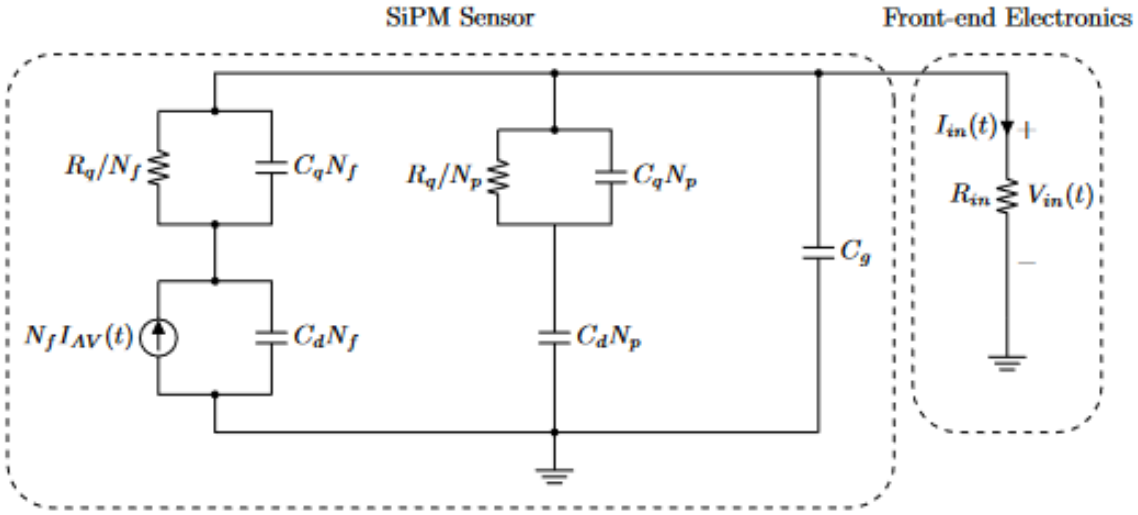


Figure 11: Corsi model[19] coupled to a generic front-end electronics[20].

An effective electrical model with accurate parameters is essential for replicating signals produced by a SiPM sensor when linked to a preamplifier. This is crucial when developing a front-end electronic system for radiation detection and conducting reliable simulations.

An improved model of a SiPM connected to front-end electronics, characterized by an input impedance $R_{in}$, is depicted in Fig.11[19]. The sensor comprises a total number of microcells $N_{tot}$, with only a subset $N_f$ becoming active during an event, while the remainder $N_p = N_{tot} - N_f$ stay inactive. The model incorporates $C_d$, the capacitance of the avalanche photodiode, $R_q$ as the quenching resistor, and $C_q$ representing the parasitic capacitance. The grid capacitance, denoted as $C_g$, arises from the interconnection of all the microcells.

When simulating the SiPM's output pulse, particularly its rising edge, an exponential current source is advisable:

$$I_{AV}(t) = I_0 e^{-t/\tau_a} \tag{1}$$

Here, $I_0$ signifies the peak current, determined by the charge from a single microcell divided by the rise time constant $\tau_a$:

$$I_0 = \frac{Q_{\mu cell}}{\tau_a} \tag{2}$$

Often, the rise of a SiPM signal is so rapid that an exact shape replication is unnecessary in practical applications[20]. In such cases, a Delta-Dirac pulse replaces the current source:

$$I_{AV}(t) = Q_{\mu cell}\delta(t) \tag{3}$$

For multiple events, due to superposition, the avalanche currents of each activated microcell can be represented by a singular current source, generating all Dirac-deltas linked to the fired microcells at different photon arrival times:

$$I_{AV}(t) = Q_{\mu cell} \sum_{i=1}^{M} \delta(t - t_i) \tag{4}$$

Parameter extraction for a SiPM sensor is complex and typically involves extensive laboratory measurements, solving sophisticated equation systems, and requires knowledge of the fabrication process, which is beyond this discussion. Therefore, the parameters of the SiPM Hamamatsu S10931-050P, with 3600 microcells each $50 \times 50\mu m$ and a total active area of $3 \times 3mm$, are utilized in the preamplifier design.

| Extracted Electrical Parameters | | Calculated Dynamic Parameters | |
|---|---|---|---|
| $Q_{\mu ph}$ | 160 fC | $\tau_F$ | $C_P \times R_{in}$ |
| $R_d$ | 1 kΩ | $\tau_S$ | $\tau_r + C_S \times R_{in}$ |
| $R_q$ | 49.6 kΩ | $\tau_d$ | 95.6 ps |
| $C_d$ | 80.14 fF | $\tau_r$ | 3.24 ns |
| $C_q$ | 15.49 fF | $I_0$ | 1.67mA |
| $C_g$ | 18.24 pF | $C_P$ | 64.9 pF |
| $N_{tot}$ | 3600 | $C_S$ | 306.7 pF |

Table 1: Electrical and Dynamic Parameters of the SiPM sensor Hamamatsu S10931-050P. Reprint from [20]

## 2.4 Comparison and Application

An inherent limitation of PMT is their tendency to deteriorate over time: their performance changes (demonstrating hysteresis) and they can incur damage from exposure to regular light(in table 2). For instance, in the context of a Cherenkov Telescope, background illumination from sources like the moon can be significant. Switching to SiPM can therefore enhance the longevity of the telescope's camera, enhance the sensitivity, higher photodetection efficiency, compactness, and robustness against magnetic fields.

Below are some applications of SiPM array dedicated readout chip:

For instance, the FLC_SIPM chip was crafted by the OMEGA group at IN2P3 for use in the ILC AHCAL[21]. Following this, the OMEGA group developed a series of ASICs suitable for SiPM array readouts, such as SPIROC[4] and MAROC[22], catering to diverse applications. The NINO chip, produced by CERN, has been implemented in the ALICE TOF experiment[23]. The University of Heidelberg designed the PETA[24] and STiC2[25] chips for PET applications. The VATA64 chip, developed by the Norwegian company Ideas, has been employed in Cherenkov ray detection experiments[26]. INFN developed the BASIC chip

| | PMT | SiPM |
|---|---|---|
| Gain | $10^5 - 10^9$ | $10^6 - 10^7$ |
| QE or PDE | Up to 40% at 415 nm | Up to 50% at 415 nm |
| Dynamic Range | Limited by the divider current | Limited by the number of micro-cells |
| Bias voltage | Up to 1000 V | Up to 60 V |
| Dark output | Up to 500 cps | Up to 1000 kcps |
| Design Complexity | High voltage | Temperature compensation |
| Mechanical Robustness | Medium | High |
| Magnetic Field | Need protection | Immune |
| Timing | Fast/Very Fast | Fast |
| Temperature Sensitivity | Low | Medium |
| Ambient Light Exposure | Can be damaged | No damage |
| Hysteresis | Yes | No |
| Warm Up Time | Required (minutes) | No |
| Price (per unit area) | High (low) | Low (high) |

Table 2: Comparison of PMT and SiPM Characteristics. Reprint from [18]

for PET applications[27], and Tsinghua University in China has created the TIMPIC[28] and EXYT[29] chips for similar purposes.

| ASIC | Year | Channels | Power Consumption | Technology | Application |
|---|---|---|---|---|---|
| FLC_SIPM | 2004 | 18 | 12 mW/channel | BiCMOS 0.8 µm | ILC AHCAL |
| NINO | 2004 | 8 | 25 mW/channel | CMOS 0.25 µm | ALICE TOF |
| MAROC2 | 2006 | 64 | 20 mW/channel | SiGe 0.35 µm | ATLAS |
| SPIROC | 2007 | 36 | 5 mW/channel | SiGe 0.35 µm | ILC AHCAL |
| PETA | 2008 | 40 | 30 mW/channel | CMOS 0.18 µm | PET |
| BASIC | 2009 | 32 | - | CMOS 0.35 µm | PET |
| VATA64 | 2009 | 64 | 16 mW/channel | CMOS 0.35 µm | Cherenkov |
| STiC2 | 2013 | 64 | 25 mW/channel | CMOS 0.18 µm | PET |
| TIMPIC2 | 2013 | 16 | 10 mW/channel | CMOS 0.35 µm | PET |
| EXYT | 2014 | 64 | 3 mW/channel | CMOS 0.18 µm | PET |

Table 3: Summary of ASICs for various applications[9].

# 3
# FRONT-END READOUT CIRCUIT

## 3.1 Architecture

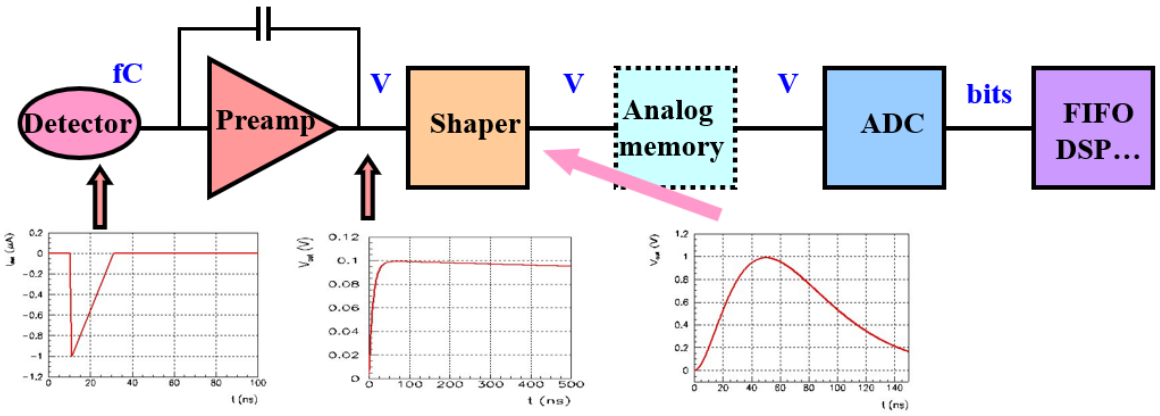


Figure 12: Architecture of front-end readout electronics. Reprint from TREX microélectronique C. de La Taille

The Fig. 12 illustrates the typical architecture of front-end electronics used in signal processing from detectors. The process flow and components are described as follows:

1. **Detector:** This is where the initial signal is received. Signals are often very small, measured in femtocoulombs (fC), and thus require amplification.

2. **Preamplifier (Preamp):** The preamplifier amplifies the tiny charge received from the detector into a more substantial voltage signal for further processing.

3. **Shaper:** Following amplification, the signal is passed through a shaper which optimizes its waveform for better measurement and analysis.

4. **Analog Memory:** Some systems include an analog memory to temporarily store the shaped analog signal before it is digitized.

5. **Analog to Digital Converter (ADC):** The ADC converts the shaped analog signal into a digital signal represented by bits.

6. **Digital Signal Processing (FIFO, DSP, etc.):** The digital signal processor further analyzes and processes the digitized signal for final readout.

## 3.2 Preamplifier

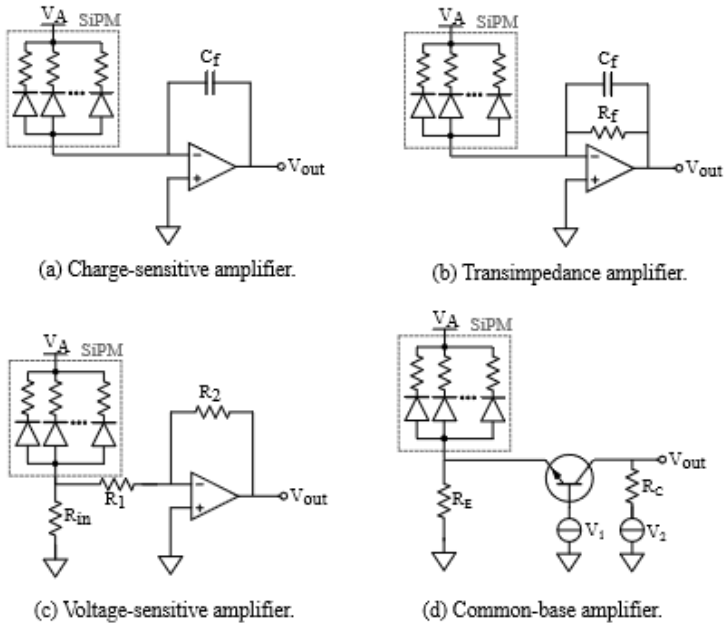


Figure 13: Schema of typical preamplifiers used to readout SiPM. Reprint from [30]

### 3.2.1 • Charge Sensitive Preamplifier

A charge-sensitive amplifier outputs a voltage that is proportionate to the integrated input current, mediated through a feedback capacitor. This type is advantageous due to its limited feedback loop impact on the timing accuracy. The equations for the associated transfer function and input impedance are provided.

$$A_{CSA} = \frac{V_{out}}{Q_{in}} = \frac{1}{j\omega C_f + \frac{1}{A_f}(C_f + C_{in})} \tag{5}$$

$$Z^{in}_{CSA} = \frac{1}{j\omega C_f (1 + A_f)} \tag{6}$$

### 3.2.2 • Transimpedance Preamplifier

Transimpedance amplifiers convert the input current into an output voltage. The input impedance of this configuration can be derived from the feedback resistance and capacitance, enhancing its bandwidth due to the feedback loop. The bandwidth and the gain-bandwidth product equations are illustrated.

$$A_{TIA} = \frac{V_{out}}{i_{in}} = -\frac{R_f}{1 + j\omega R_f C_{in}(1 + \beta)} \tag{7}$$

where $\beta = \frac{1}{1+j\omega R_f C_{in}}$. Its bandwidth can be approximated by:

$$BW_{TIA} = \frac{GBW}{2\pi R_f C_{in}} \tag{8}$$

where $GBW$ is the gain bandwidth product of the amplifier.

### 3.2.3 • Voltage Sensitive Preamplifier

Voltage-sensitive amplifiers output a voltage corresponding to the input. They offer a better dynamic range and occupy less space compared to charge-sensitive variants. The associated transfer function for this type of preamplifier, which considers the sensing resistor and other components, is presented.

$$A_{VA} = \frac{V_{out}}{V_{in}} = -\frac{A_f R_f}{(1 + A_f R_f)R_f + R_2} \tag{9}$$

with $V_{in} = i_{in} R_{in}$.

### 3.2.4 • Current Buffer

Current buffers are implemented to interface between the current and voltage domains without requiring multiple conversions. The input impedance and the transfer function for a current buffer configuration are described.

$$A_{CBA} = \frac{V_{out}}{i_{in}} = 1 \text{ if } \beta >> 1, \tag{10}$$

and the input impedance is approximated by:

$$Z^{in}_{CBA} = r_e(\sim \frac{1}{g_m}) \text{ if } \beta >> 1. \tag{11}$$

First we use a common source amplifier in Fig. 14. In this structure, R0 and R3 are bias resistors. They help set the operating point of the transistor and ensure that the transistor operates in the correct amplification region. Vdc is the supply voltage that provides the required DC power to this amplifier.

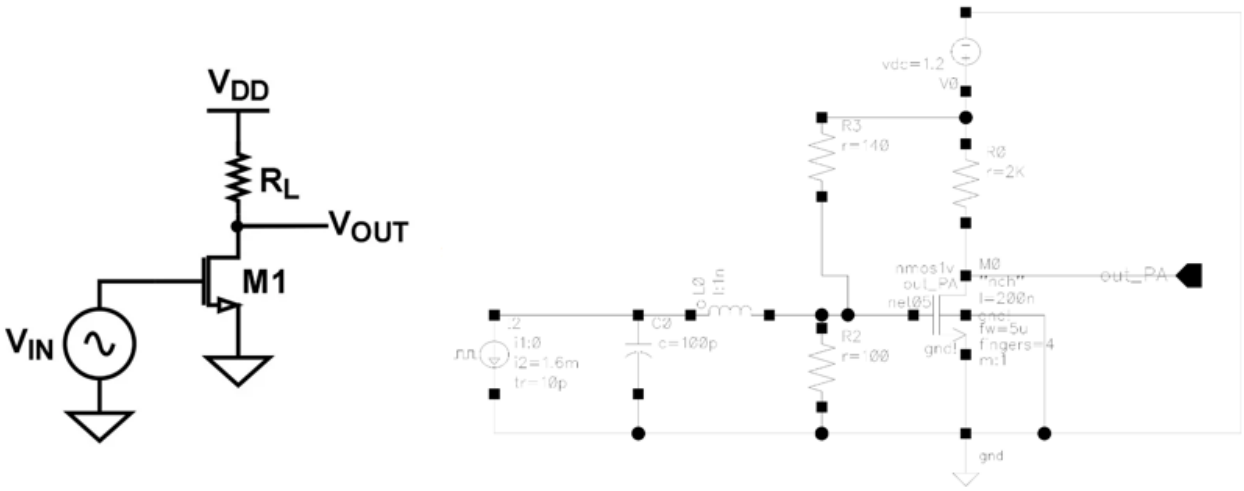


Figure 14: Schema of common source amplifier.

$$\text{Gain} = \frac{\Delta V_{\text{output}}}{\Delta V_{\text{input}}} = \frac{-13 \text{ mV}}{1.75 \text{ mV}} \approx -7.43 \tag{12}$$

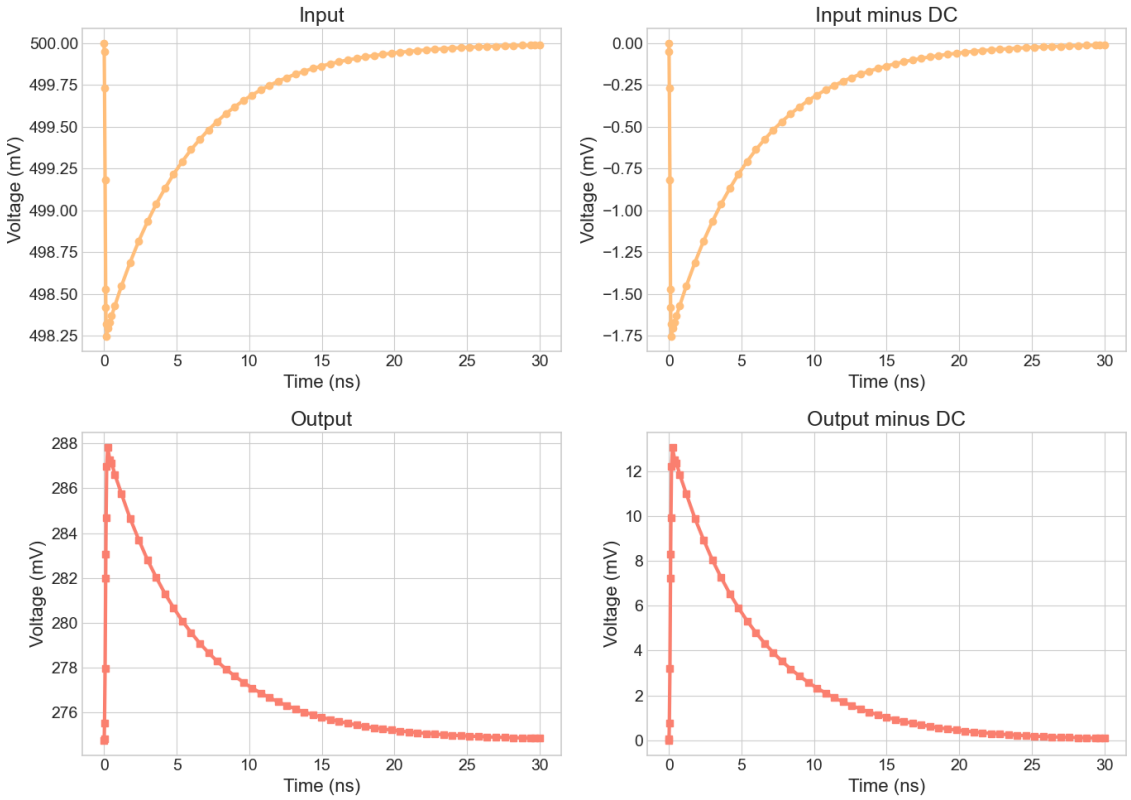


Figure 15: Input and output of common source amplifier.

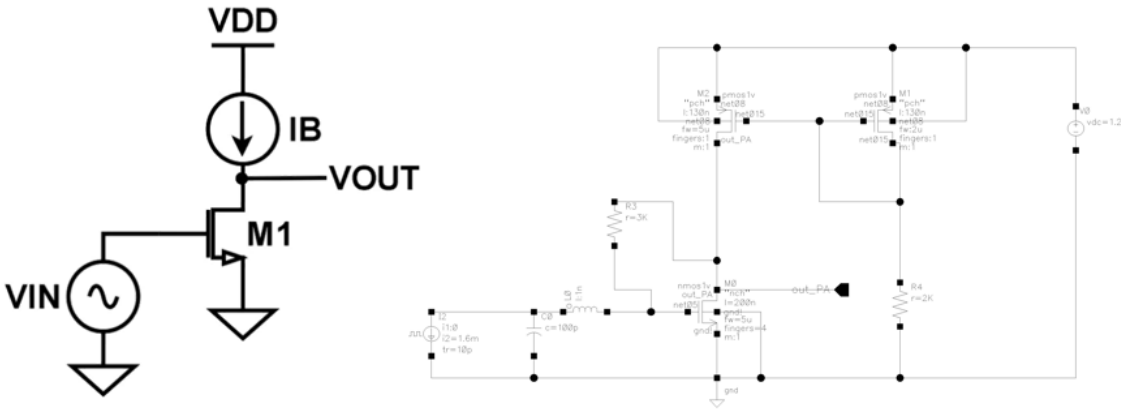


Figure 16: Schema of common source amplifier with current source.

We change the resistor into a current source, and since an ideal current source doesn't actually exist, we use a current mirror to replicate the current.

$$\text{Gain} = \frac{\Delta V_{\text{output}}}{\Delta V_{\text{input}}} = \frac{-14\ \text{mV}}{1.75\ \text{mV}} = -8 \tag{13}$$

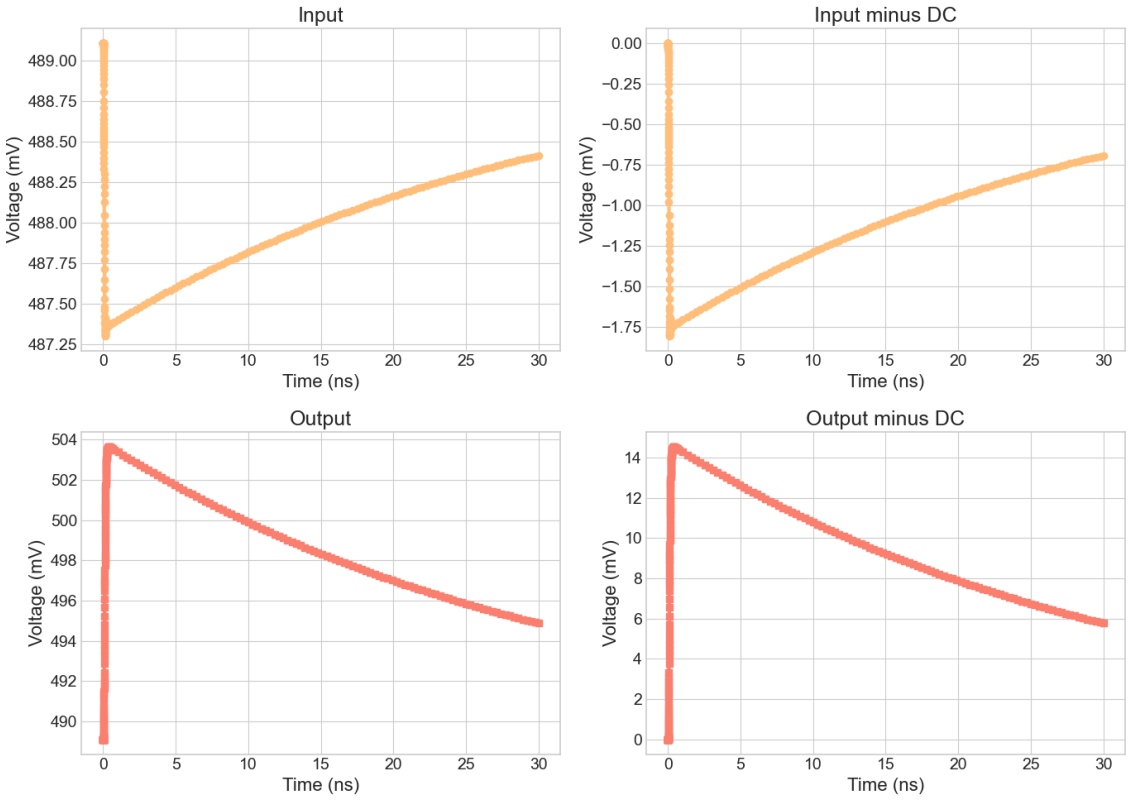


Figure 17: Input and output of common source amplifier with current source.

## 3.3 Discriminator

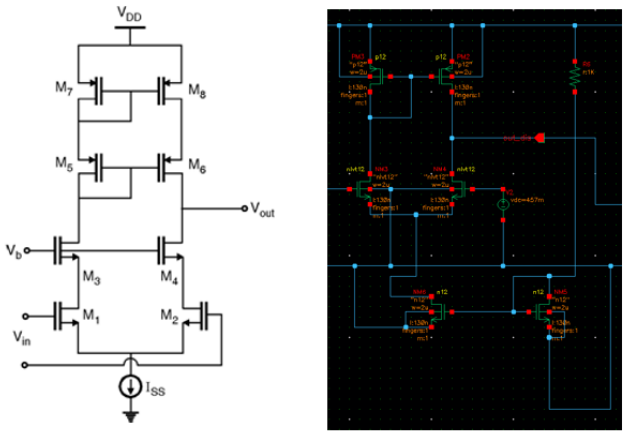


Figure 18: (Left)Cascode differential amplifier. (Right) Simplified discriminator

As indicated in Fig. 18, we use a simple cascode differential amplifier with an amplified signal on one end (with DC voltage 447mV) and the other end set to a suitable constant voltage (457mV), so once the signal comes, the voltage rises above the threshold voltage and we get an amplified output signal(Fig. 19).

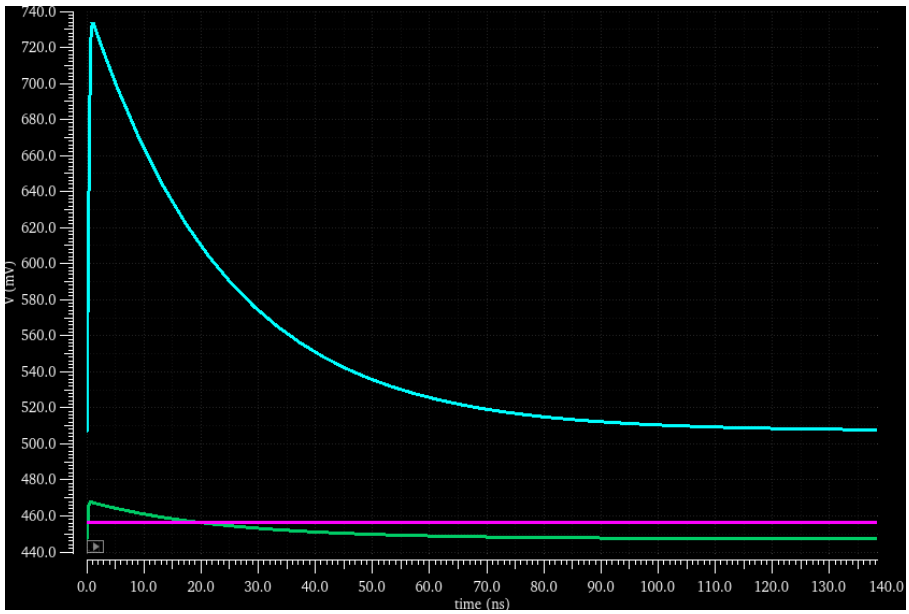


Figure 19: Green is the input signal, purple is the threshold voltage, and blue is the output signal.

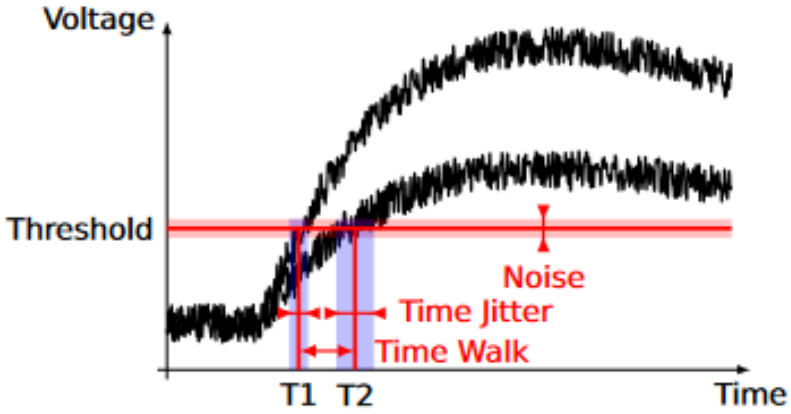


Figure 20: Timing errors with leading edge discrimination.

Fig. 20 illustrates the two sources of timing error for leading edge discrimination: time walk and time jitter. Time walk refers to timing variations that occur due to differences in signal amplitudes. The discrimination threshold is typically set above the baseline of the SiPM to prevent noise from triggering it. Time jitter represents the statistical time stamp fluctuations caused by system noise. The time jitter, denoted as $\sigma_t$, is given by:

$$\sigma_t = \frac{\sigma_v}{\left|\frac{dV(t)}{dt}\right|} = \frac{1mV}{\left|\frac{0.2mV}{2pS}\right|} = 10pS \tag{14}$$

where $\sigma_v$ is the total noise in the system, and $\left|\frac{dV(t)}{dt}\right|$ is the slope of the SiPM signal at the discrimination point.

Various sources contribute to the total system noise $\sigma_v$, such as the statistical fluctuation of charge carrier creation and initiation of the avalanche, the fluctuation of avalanche buildup process, as well as the noise on the quenching resistor and in the readout electronics. The baseline fluctuation due to the pile-up effect of dark count noise also contributes to $\sigma_v$ and degrades the time jitter at high bias voltages.

The slope $\left|\frac{dV(t)}{dt}\right|$ is influenced by the speed of the avalanche development, the detector parasitic, the bandwidth of the readout electronics, and the number of photons that arrive at the sensor surface before the discrimination time. The phenomenon where a discriminator generates a signal even though the input signal has not reached the specified threshold voltage is typically due to what's known as an "offset" in the discriminator. This deviation can be caused by several factors, such as manufacturing imperfections, thermal noise, or variations in supply voltage.

## 3.4 Analog-to-digital converter

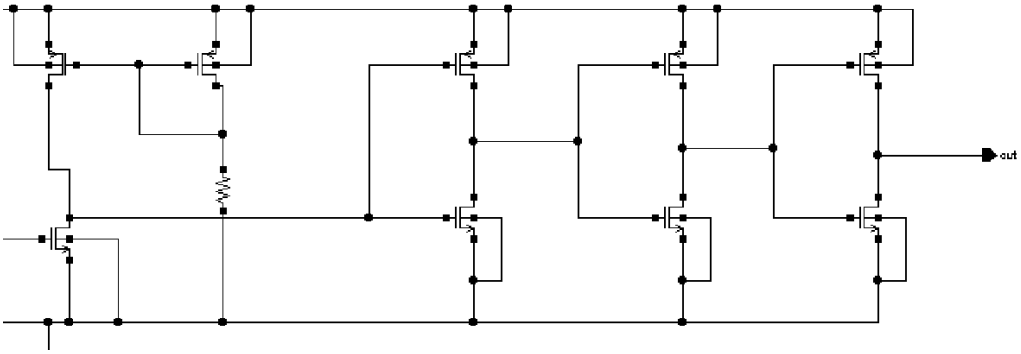


Figure 21: Schematic of ADC.

Afterwards, the signal output from the discriminator is set to turn on an NMOS, so that the output signal increases and bottoms out close to 0 mV in Fig. 22. This signal is then passed through three inverters, and finally we get a clear digital signal (from 0V to 1.2V) in Fig. 23.

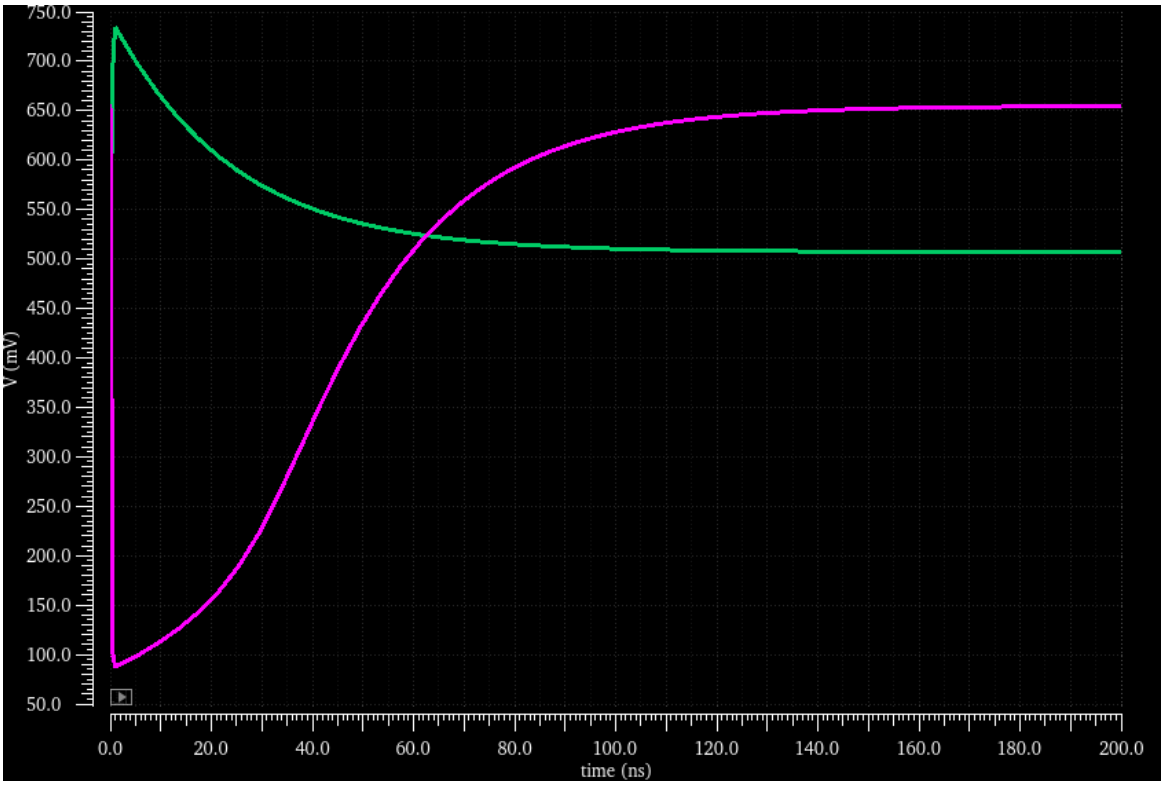


Figure 22: Output of discriminator(green) and output of NMOS(purple).

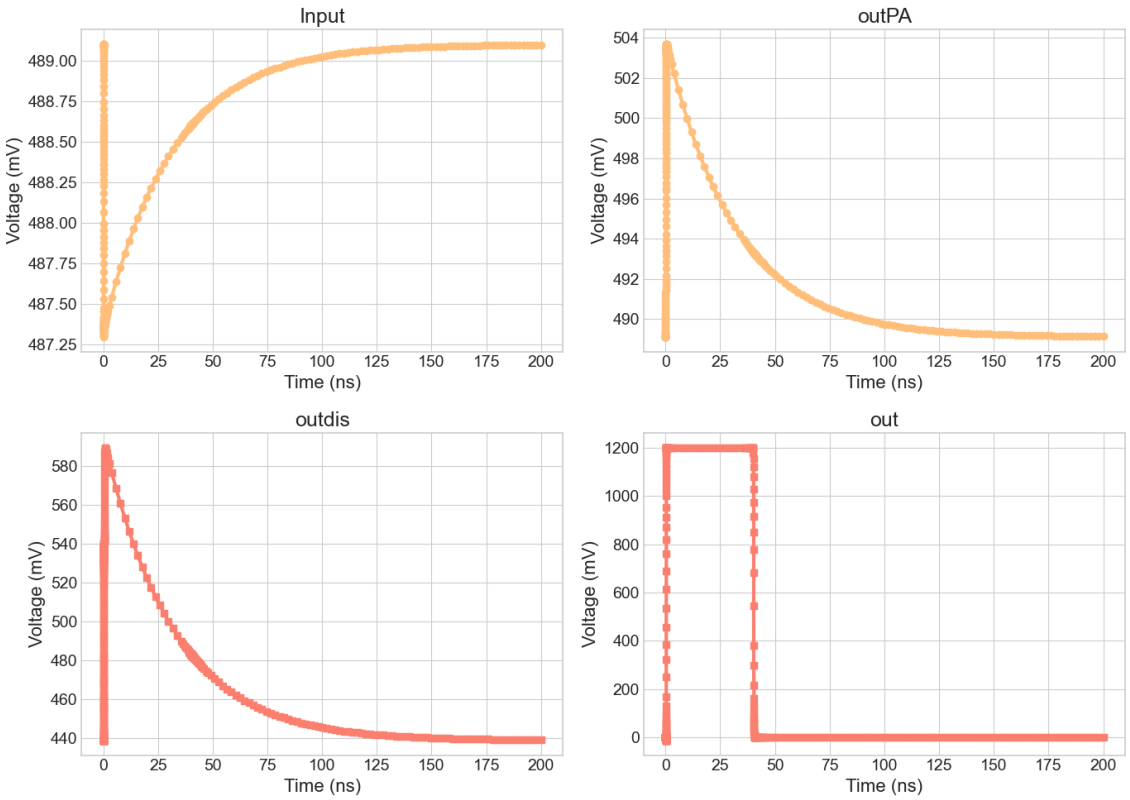


Figure 23: Input, output of preamp, output of discriminator and output.

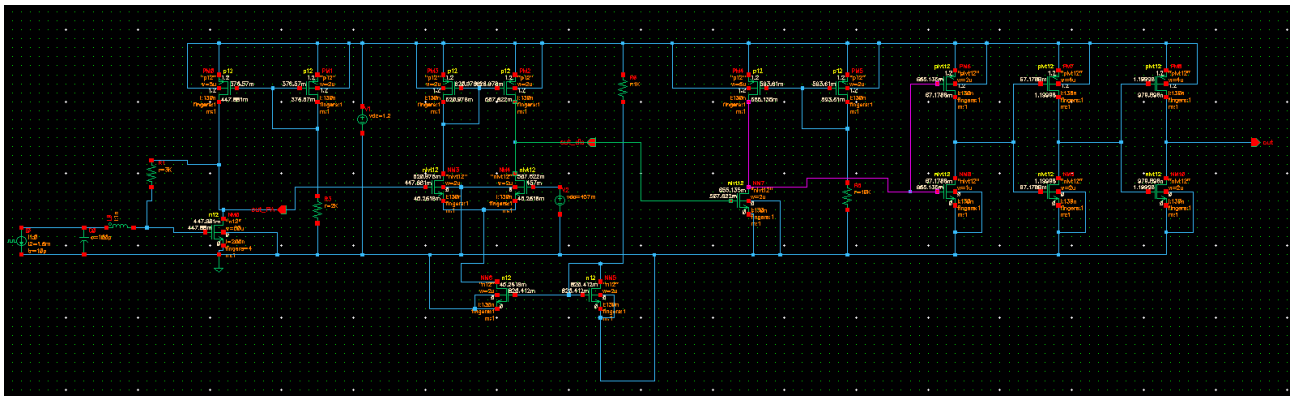

Figure 24: Final schematic.

# 4 CMOS LAYOUT DESIGN AND VERIFICATION

Layout process is the step where the abstract schematic representation of the circuit is translated into a physical layout, which maps out the exact placement of transistors and interconnections on the silicon wafer.

## 4.1 Design Rule Checking (DRC)

The Design Rule Checking (DRC) is one of the most critical steps in the layout process. DRC is an automated process that verifies the layout to ensure compliance with the predefined design rules of the fabrication process. These design rules are a set of parameters provided by the semiconductor foundry, which includes minimum widths for the transistors and wires, minimum spacing between different features, and other geometric and procedural constraints. The purpose of DRC is to check for violations of these rules that could lead to manufacturing defects, ensuring the manufacturability of the design.

## 4.2 Layout Versus Schematic (LVS)

Following DRC, the Layout Versus Schematic (LVS) check is performed. LVS is a verification step to confirm that the physical layout accurately reflects the original schematic diagram in terms of connectivity and functionality. This step involves extracting the netlist from the layout and comparing it against the schematic netlist.

The version we have designed is shown below:

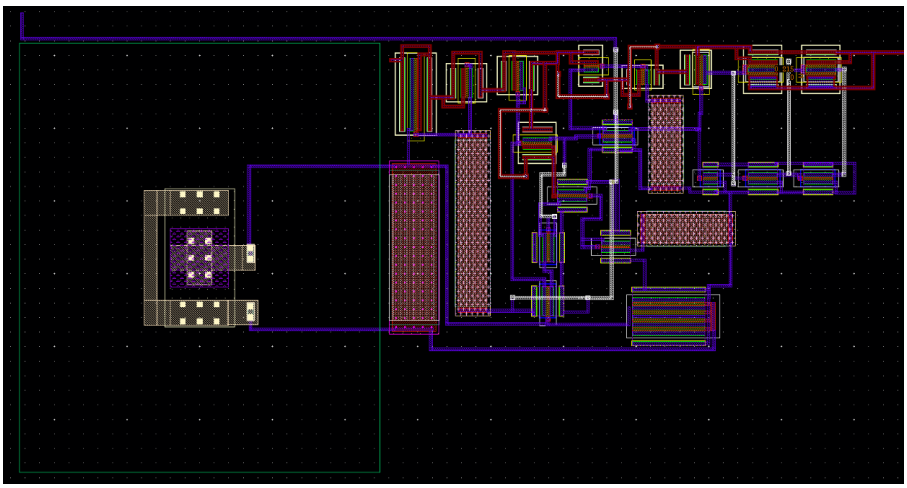

Figure 25: Layout of the analog front end.

## 4.3 Parasitic Extraction

After ensuring the physical layout matches the schematic, the next step is parasitic extraction. This process involves identifying and measuring the parasitic capacitances, resistances, and inductances that inherently exist within the layout due to the physical configuration of the interconnects and transistors. These parasitic elements can significantly affect the performance of the IC, particularly at higher frequencies, by introducing unwanted signal delays, crosstalk, and power dissipation.

Parasitic extraction tools analyze the layout to quantify these unwanted effects and produce a parasitic netlist that supplements the ideal circuit netlist. This enriched netlist allows for more accurate post-layout simulation to validate the performance of the IC under realistic conditions, which includes the effect of the parasitics. Addressing the impact of parasitic elements is crucial for high-speed and RF circuits, where they can severely degrade signal integrity and overall functionality. Here is the testbench we design in order to perform post layout simulation:

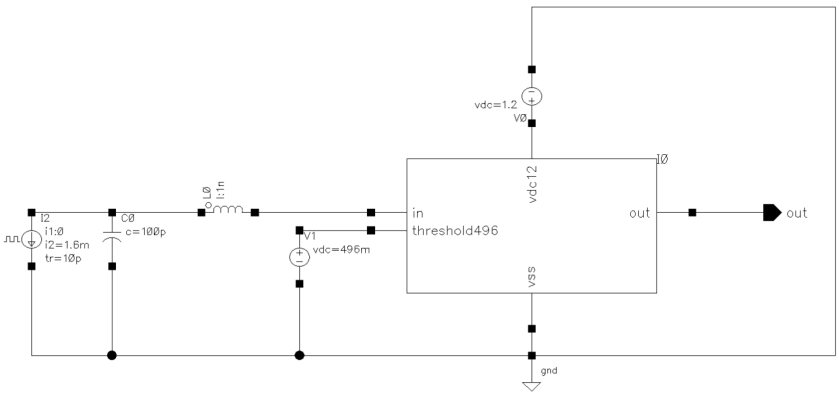


Figure 26: Testbench for post layout simulation.

## 4.4 Post layout simulation

This simulation uses the layout-extracted netlist, including the parasitics, to model and analyze the behavior of the IC in a virtual environment that more closely mirrors real-world conditions.

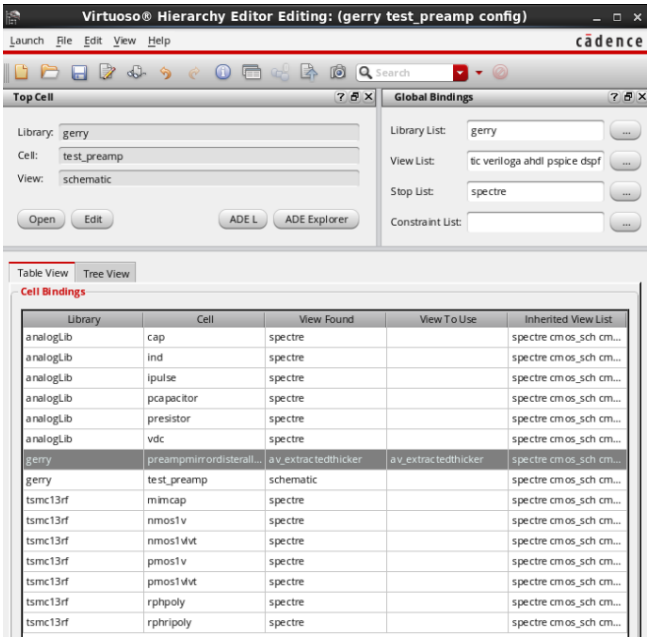


Figure 27: Setting for post layout simulation.

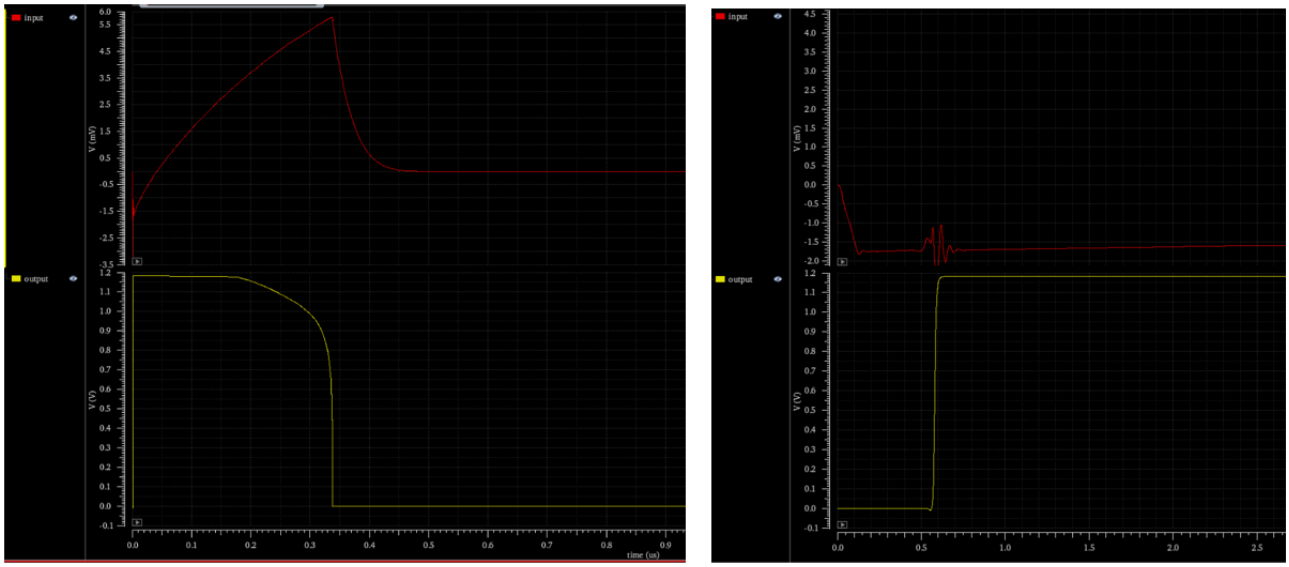


Figure 28: Input and output signal.

From the Fig. 28, it can be found that the input signal has been seriously distorted, the signal input can only rise to 0.5mV after falling from 0mV, and the length of the signal time reaches 300ns, the size of which is seriously smaller than that of the normal signal of 3mV, while the time is much larger than that of the normal signal of 30ns.

We extract only the parasitic parameters of the capacitor for simulation as Fig.29 The input and output signals are found to be normal. It can therefore be deduced that it is due

to the metal wires of Vdd and Vss in the plate being too narrow (0.16 $\mu$m) resulting in a high resistance, which in turn prevents the signal from rising, and therefore the Vdd and Vss in the layout are thickened to about 1 $\mu$m and then post imitated.

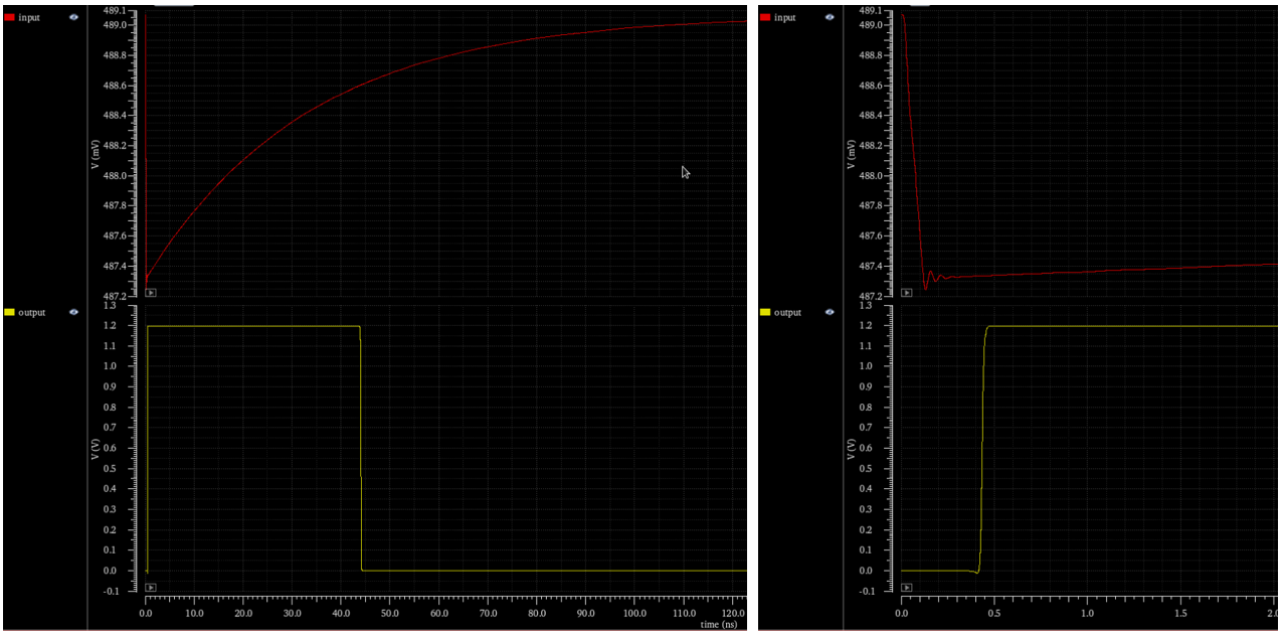


Figure 29: Input and output signal with only capacitor extracted.

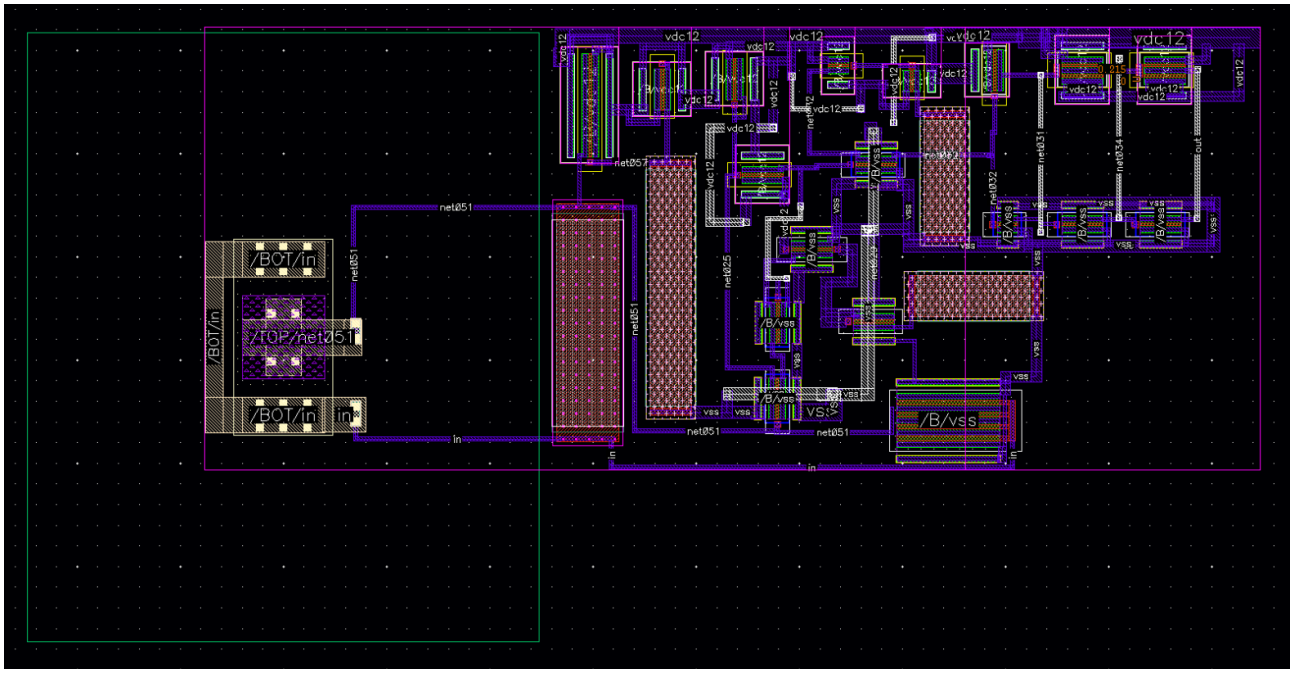


Figure 30: Layout with thicker Vdd and Vss.

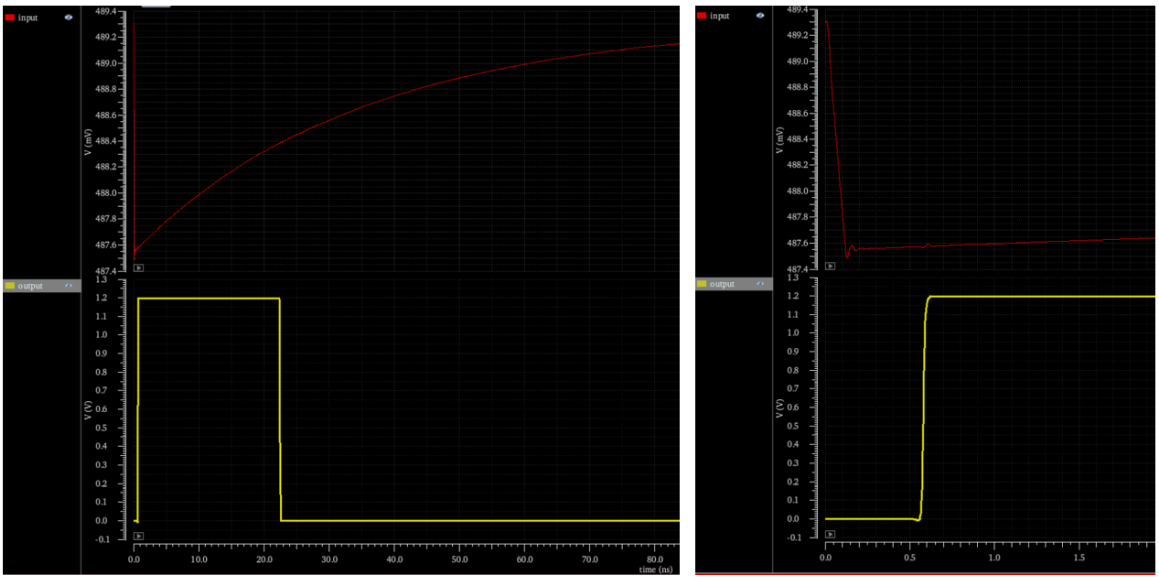


Figure 31: Input and output signal with thicker Vdd and Vss.

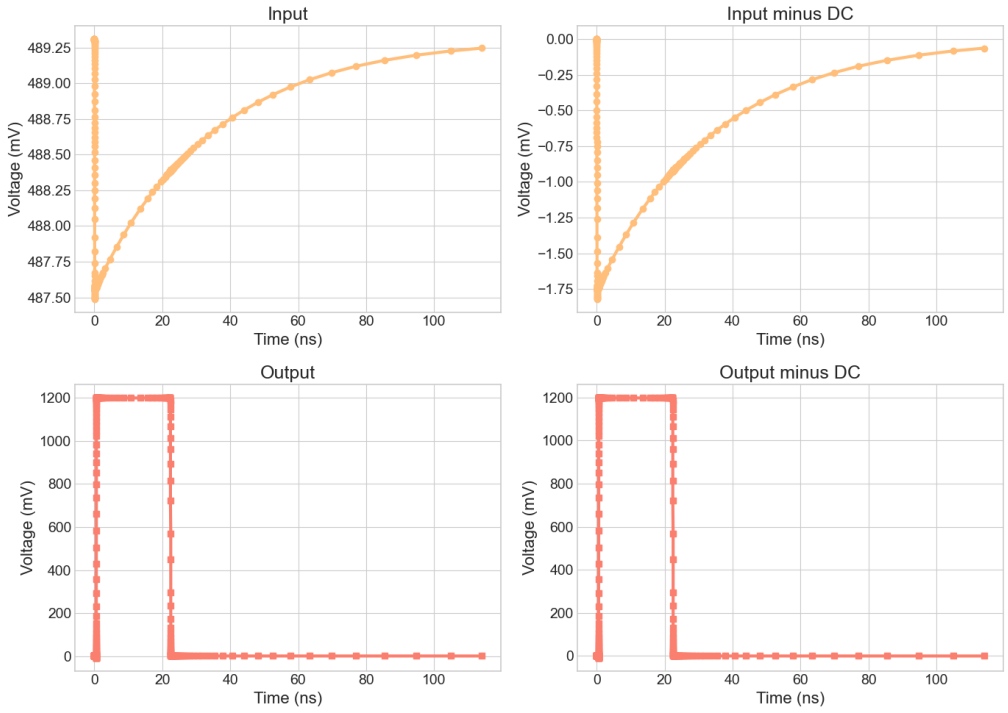


Figure 32: Input and output signal with thicker Vdd and Vss.

From the Fig. 31 and 32, it can be seen that by widening the metal line and lowering the resistance, the amplitude of the oscillation of the signal at the bottom is reduced and its recovery time is accelerated, and the width of the digital signal is reduced from 44ns to 23ns, which is conducive to a better identification of the particles.

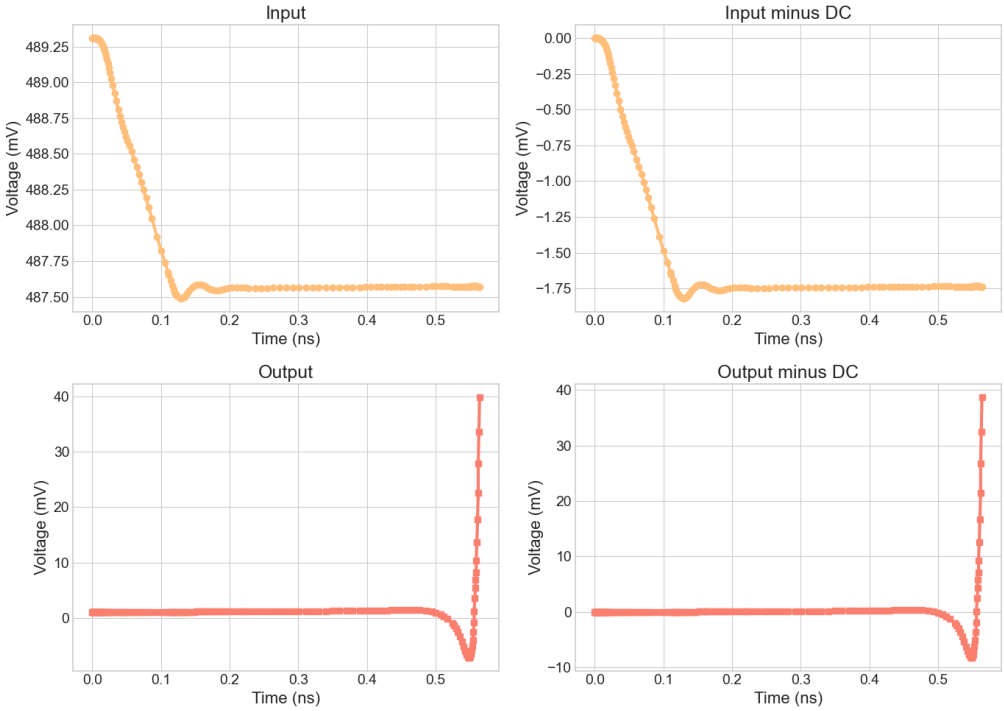


Figure 33: Input and output signal with thicker Vdd and Vss within 0.5ns.

# 5 CONCLUSIONS

Thanks very much for PHY581C - Microelectronics Experimental ASIC Design, the Professor Christophe De la taille taught us how to design a front-end readout circuit for SiPM by hand. Through design, simulation, and verification processes, including essential steps like Design Rule Checking (DRC), Layout Versus Schematic (LVS), and parasitic extraction, we has learnt how to transfer theoretical models into practical, efficient electronic designs.

In this process, through the teacher's hands-on guidance, I learned a very valuable experience, from the MOS tuning parameter to the layout design of the Layout to the troubleshooting of each process such as the analysis of the netlist error in the LVS, and finally the source of the signal distortion problem.

It is also understood that in analogue integrated circuit design, there is still a lot of knowledge to be learnt and there is a lot that can be optimised in this design. Circuit mismatch usually refers to a situation where the actual physical and electrical characteristics of a circuit component do not exactly match the design specifications due to unavoidable errors in the manufacturing process. For example, in a current mirror, two theoretically identical MOS tubes will have slight differences in their dimensions (width W and length L) due to process errors, resulting in a mismatch in the current Iout flowing through them, which is the reason for the difference in DC bias.

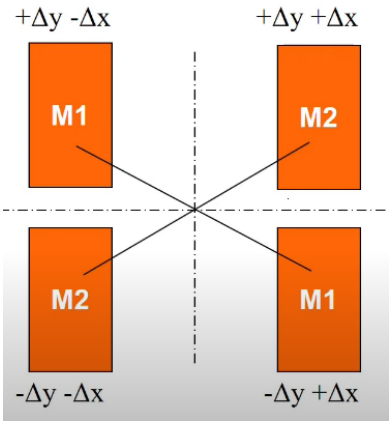


Figure 34: Device matching.

To cope this problem, we can divide the matching transistors into cells (fingers) and lay them out on the wafer in a symmetrical manner. In the case of a current mirror, the designer might split the two MOS transistors that make up the current mirror into smaller units and arrange them crosswise to form a symmetrical pattern. In this way, process fluctuations affect each transistor more consistently, even in different areas of the wafer, which reduces mismatches in Fig.34. In addition, we can use more complex amplification and current mirror structures for better performance, filtering of noise, and designing more channels[31], as well as modularity

in the design so that we can better analyse the source of the problem when extracting parasitic parameters in the layout.

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